CLAIMS

What is claimed is:

1. A multiplexed address and data bus controlled by a bus master for communication between two microprocessors, comprising:

a plurality of multiplexed address and data lines in communication between the two microprocessors;

a read/write control signal line in communication between the two microprocessors for communicating whether a read or a write operation is to be performed;

a chip select line in communication between the two microprocessors, said chip select line transitioning to an enable condition during a data transfer cycle; and

a data strobe line in communication between the two microprocessors, said data strobe line providing a plurality of signals for each data transfer cycle wherein each data transfer cycle includes a plurality of write and read sequences which are initiated by said signals from said data strobe line.

2. The multiplexed address and data bus according to claim 1, wherein said plurality of write and read sequences include an address transfer sequence and at least one data transfer sequence.

3. A method of multiplexed address and data transfer for communicating between two microprocessors, comprising the steps of:

providing a chip select strobe signal to initiate a data transfer cycle and maintaining said chip select strobe signal during a duration of said data transfer cycle;

providing a read/write line qualifier signal to identify whether a read or a write data transfer operation is to be performed; and

providing a data strobe signal that steps one of the microprocessors through the data transfer cycle.

4. The method according to claim 3, wherein the data transfer includes address information which is transferred during a first data strobe and at least one data string that is transferred during subsequent data strobes.